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## **AMENDMENTS TO THE CLAIMS**

1. (Currently Amended) A subsystem for use in a wireless local area networking device, comprising:

a transceiver:

programmable gates coupled to the transceiver; [[and]]

memory coupled to the programmable gates, the memory storing instructions for programming a first portion of the programmable gates as a selected one of a first type of [[a]] medium access layer and a second type of [[a]] medium access layer, the first type of [[the]] medium access layer different from the second type of [[the]] medium access layer, wherein the first type of [[the]] medium access layer and the second type of [[the]] medium access layer are compatible with the transceiver, the memory storing instructions for programming a second portion of the programmable gates as a baseband controller;

the transceiver being coupled to the programmable gates through programmable input/output blocks;

the transceiver and the programmable gates being formed as an integrated circuit; and

the first type of medium access layer and the second type of medium access layer having a common access to the transceiver.

## Claim 2. (Cancelled)

3. (Currently Amended) The subsystem of claim 1 wherein the first type of medium access control layer comprises a Carrier Sense Multiple Access protocol, and the second type of medium access control layer comprises a Time Division Multiple Access protocol.

## Claim 4. (Cancelled)

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5. (Currently Amended) The subsystem of claim [[4]] 1 wherein the integrated circuit is a Field Programmable Gate Array.

- 6. (Original) The subsystem of claim 1 wherein the memory stores instructions for programming a third portion of the programmable gates as a baseband processor.
- 7. (Currently Amended) A subsystem for use in a wireless local area network device, comprising:

a transceiver;

programmable gates coupled to the transceiver; [[and]]

memory coupled to the programmable gates, the memory storing instructions for programming a first portion of the programmable gates with a selected one of a first data-link layer and a second data-link layer, the first data-link layer different from the second data-link layer, wherein the first data-link layer and the second data-link layer are compatible with the transceiver, the memory storing instruction for programming a second portion of the programmable gates with a baseband controller;

the transceiver, the programmable input/output blocks, and the programmable gates being formed as an integrated circuit; and

the first data-link layer and the second data-link layer having a common access to the transceiver.

- 8. (Original) The subsystem of claim 7 further comprising a baseband processor coupled to the programmable gates.
- 9. (Original) The subsystem of claim 8 wherein the transceiver and the baseband processor are coupled to the programmable gates through programmable input/output blocks.

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10. (Original) The subsystem of claim 9 wherein the first data-link layer comprises a first logical link control sub-layer and a first medium access control sub-layer, and the second data-link layer comprises a second logical link control sub-layer and a second medium access control sub-layer.

- 11. (Original) The subsystem of claim 10 wherein the first medium access control sub-layer comprises a Carrier Sense Multiple Access protocol, and the second medium access control sub-layer comprises a Time Division Multiple Access protocol.
  - 12. (Original) A circuit board, comprising:

a field programmable gate array comprising programmable configuration logic blocks and programmable input/output blocks coupled to the programmable configuration logic blocks;

a radio coupled to the programmable configuration logic blocks through the programmable input/output blocks;

program memory coupled to the programmable configuration logic blocks through the programmable input/output blocks;

data memory coupled to the programmable configuration logic blocks through the programmable input/output blocks; and

an interface transceiver coupled to the programmable configuration logic blocks through the programmable input/output blocks;

the program memory comprising programming instructions for the programmable configuration logic blocks to be configured as,

a radio interface and controller;

a medium access control protocol engine and configuration controller; and

a baseband processor interface.

13. (Original) The circuit board of claim 12 wherein the program memory comprises programming instruction for the programmable configuration logic blocks to

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be configured as a baseband processor.

14. (Original) The circuit board of claim 12 wherein the program memory comprises programming instruction for the programmable configuration logic blocks to be configured as an encryption engine.

- 15. (Original) The circuit board of claim 12 wherein the program memory comprises programming instruction for the programmable configuration logic blocks to be configured as a memory controller and host bus interface.
- 16. (Original) The circuit board of claim 12 wherein the program memory comprises programming instruction for the programmable configuration logic blocks to be configured as a memory controller, host device interface and host device controller.
- 17. (Original) The circuit board of claim 16 wherein the host device interface and the host device controller are user selectable.

Claims 18-24. (Cancelled)